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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/806,350 | 03/23/2004 | Hiroshi Mizuhashi | OKI.647 | 3991 |
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20987 7590 10/20/2006

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EXAMINER

PHAN, TRONG Q

| ART UNIT | PAPER NUMBER |
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2827

DATE MAILED: 10/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | | |
|------------------------------|-------------------------------|------------------------------------|--|
| Office Action Summary | Application No. 10/806,350 | Applicant(s) MIZUHASHI, HIROSHI | |
| | Examiner TRONG PHAN | Art Unit 2827 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 August 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☐ Claim(s) _____ is/are rejected.
- 7) ☒ Claim(s) 1-18 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Upon reconsideration, the Final Office Action of 2/22/06 has been withdrawn.

A new non-FINAL Office Action has been set forth as follow:

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: PY0_1_2[0:7], PY3_4[0:3], PY5_6[0:3], PY7_8[0:3], PY1_2D[0:7], PY3_4D[0:3], PY5_6D[0:3] and PY7_8D[0:3] in Figs. 1 and 5; TGR(L), k and ℓ in Fig.4; tCYC, TGR(L), k and ℓ in Fig. 7. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities:

Regarding Fig. 3 of the present invention:

It is not understood what “a voltage drop caused by threshold voltage of the transistors” (last line of page 6) really is since there are so many transistors in Fig. 3 and the specification does not define any specific transistor to bear a voltage drop caused by a threshold voltage of the transistors.

It is not understood how the another sense amplifier 301 in another memory cell block 19 can be **connected** to a bit line pair BL[j] and BLb[j] in response to the “H” level of the block selecting signal YBSEL[i] and the column selecting signal Y[j] as described in lines 2-6, page 9 of the specification. Because, first of all, how the Ith of block selecting signal YBSEL[i] is incorporated with the jth not the Ith of column selecting signal Y[j] and, secondly, as defined in lines-14, page 8 of the specification, when the column selecting signal Y is changed to the “H” level, the N-channel MOS transistors 222 and 223 are turned ON to connect sense amplifier 301 to the data buses DB and DBb and the sense amplifier 301 is **disconnected** from the bit line pair BL and BLb.

It is not understood how the data latching operation in the sense amplifier 301, which is connected to the bit line pair BL[j] and BLb[j], is selected by the column selecting signal Y[j] as described in lines 11-15, page 9 of the specification. Because the specification defines in lines 6-14, page 9 that column selecting signal Y is used for selecting the corresponding ON transistors 222 and 223 of the data bus connection circuit 307 in order to connect the sense amplifier 301 to the data bus DB and DBb while the sense amplifier disconnected from the bit line pair BL and BLb.

Regarding Fig. 4 of the present invention:

It is not understood what elements TGR(L), k and ℓ really are since they are not described in the specification; the operating relationship between the signal waveforms CLK, BURST, WDE, DBEQ and with respect to signal waveforms YBSEL, TGR(L), Y[i] and Y[j] are not described in the specification.

Regarding Fig. 6 of the present invention:

It is not understood how the another sense amplifier 301 in another memory cell block 19 can be **connected** to a bit line pair BL[j] and BLb[j] in response to the "H" level of the block selecting signal YBSEL[l] and the column selecting signal Y[j] as described in lines 11-13, page 12 of the specification. Because, first of all, how the lth of block selecting signal YBSEL[l] is incorporated with the jth not the lth of column selecting signal Y[j] and, secondly, as defined in lines-14, page 8 of the specification, when the column selecting signal Y is changed to the "H" level, the N-channel MOS transistors 222 and 223 are turned ON to connect sense amplifier 301 to the data buses DB and DBb and the sense amplifier 301 is **disconnected** from the bit line pair BL and BLb.

It is not understood how the data latching operation in the sense amplifier 301, which is connected to the bit line pair BL[j] and BLb[j], is selected by the column selecting signal Y[j] as described in lines 19-22, page 12 of the specification. Because the specification defines in lines 6-14, page 9 that column selecting signal Y is used for selecting the corresponding ON transistors 222 and 223 of the data bus connection circuit 307 in order to connect the sense amplifier 301 to the data bus DB and DBb while the sense amplifier disconnected from the bit line pair BL and BLb.

Regarding Fig. 7 of the present invention:

It is not understood what elements tCYC, TGR(L), k and ℓ really are since they are not described in the specification; the operating relationship between the signal waveforms CLK, BURST, WDE, DBEQ and with respect to signal waveforms YBSEL, TGR(L), Y[i] and Y[j] are not described in the specification;

The change from VPP level down to VDD level of signal waveform TGR(L) is not described in the specification.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-5, 6-10 and 12-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, a data line and a first bit line are not readable on the respective Figs. 3 and 5 of the present invention since there are data lines DB and DBb and bit lines BL and BLb shown in Figs. 3 and 5; the step of connecting the data line to a second sense amplifier when the first bit line is connected to the first sense amplifier (last paragraph) is not seen to be described in the specification. The specification only describes the latching next data operation in another second sense amplifier 301, which is connected to a bit line pair BL[j] and BLb[j], while the writing operation from the first sense amplifier

301 to the bit lines pair BL[i] and BLb[i] performed (see lines 4-8, page 9). The latching operation is performed only when the data line pair DB and DBb are disconnected (not connected) to sense amplifier 301. It is also noted that when the bit lines are connected to the sense amplifier 301 to start the latching operation, the data lines are disconnected from the sense amplifier 301 and the transfer gates 302/302 in all memory cell blocks in Fig. 3 of the present invention are all controlled by the same respective signals TGL, TGLb, TGR and TGRb and the transfer gates 607/608 in all memory cell blocks in Fig. 5 of the present invention are all controlled by the same respective signals TGL and TGR, therefore, the bit lines in all memory cells blocks in Figs. 3 and 5 of the present invention must be turned ON simultaneously at the same time while the data lines is disconnected from the sense amplifier and must be turned OFF simultaneously at the same time while the data lines is connected to the sense amplifier 301.

Specifically, whenever the data line is selectively connected to any sense amplifier 301 in any memory cell blocks by column selecting signal Y, all the bit lines BL and BLb in all memory cell blocks must be consistently turned OFF. The data line can not be connected to a second sense amplifier when the bit line is connected to the first sense amplifier as claimed.

Claim 2 is not readable on the respective Figs. 3 and 5 of the present invention because there are Y, TGL, TGLb, TGR and TGRb signals to control the recited connections in Figs. 3 and there are Y[j], TGL and TGR signals to control the recited connections in Figs. 6; the data line and the first bit line are not readable on the

respective Figs. 3 and 5 of the present invention since there are data lines DB and DBb and bit lines BL and BLb shown in Figs. 3 and 5.

Claim 3, the data line and a second bit line are not readable on the respective Figs. 3 and 5 of the present invention since there are data lines DB and DBb and bit lines BL and BLb in the next second memory cell block shown in Figs. 3 and 5.

Claim 4, the second bit line are not readable on the respective Figs. 3 and 5 of the present invention since there are bit lines BL and BLb in the next second memory cell block shown in Figs. 3 and 5.

Claim 5, the first bit line are not readable on the respective Figs. 3 and 5 of the present invention since there are bit lines BL and BLb in the first memory cell block shown in Figs. 3 and 5.

Claim 7, the first bit line are not readable on the respective Figs. 3 and 5 of the present invention since there are bit lines BL and BLb in the first memory cell block shown in Figs. 3 and 5; the feature "the switching transistor is driven be a first voltage and then driven by a second voltage which is higher than the first voltage" are not seen to be described in the specification as well as to be shown in the drawings of the present invention.

Claim 8, a data line, a first bit line and a second bit line are not readable on the respective Figs. 3 and 5 of the present invention since there are data line pair DB and DBb, first bit lines BL and BLb and second bit lines BL and BLb in the next memory cell block shown in Figs. 3 and 5; all the recited steps of transferring are not seen to be described in the specification as well as in the drawings of the present invention; the

step of transferring the second data from the second sense amplifier to a second bit line after the second sense amplifier is disconnected from the data line is not seen to be described in the specification as well as to be shown in the drawings of the present invention. The specification only describes the latching next data operation in another second sense amplifier 301, which is connected to a bit line pair BL[j] and BLb[j], while the writing operation from the first sense amplifier 301 to the bit lines pair BL[i] and BLb[i] performed (see lines 4-8, page 9). The latching operation is performed only when the data line pair DB and DBb are disconnected (not connected) to sense amplifier 301. It is also noted that when the bit lines are connected to the sense amplifier 301 to start the latching operation, the data lines are disconnected from the sense amplifier 301 and the transfer gates 302/302 in all memory cell blocks in Fig. 3 of the present invention are all controlled by the same respective signals TGL, TGLb, TGR and TGRb and the transfer gates 607/608 in all memory cell blocks in Fig. 5 of the present invention are all controlled by the same respective signals TGL and TGR, therefore, the bit lines in all memory cells blocks in Figs. 3 and 5 of the present invention must be turned ON simultaneously at the same time while the data lines is disconnected from the sense amplifier and must be turned OFF simultaneously at the same time while the data lines is connected to the sense amplifier 301. Specifically, whenever the data line is selectively connected to any sense amplifier 301 in any memory cell blocks by column selecting signal Y, all the bit lines BL and BLb in all memory cell blocks must be consistently turned OFF. The second data from data line can not be transferred to a

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second sense amplifier when the first bit line is connected to the first sense amplifier as claimed.

Claim 9, the second bit line are not readable on the respective Figs. 3 and 5 of the present invention since there are bit lines BL and BLb in the next second memory cell block shown in Figs. 3 and 5.

Claim 10, the first bit line are not readable on the respective Figs. 3 and 5 of the present invention since there are bit lines BL and BLb shown in Figs. 3 and 5.

Claim 12, the first bit line are not readable on the respective Figs. 3 and 5 of the present invention since there are bit lines BL and BLb shown in Figs. 3 and 5; the feature "the switching transistor is driven be a first voltage and then driven by a second voltage which is higher than the first voltage" is not readable on the respective drawings of the present invention.

Claim 13, a data line and a first bit line are not readable on the respective Figs. 3 and 5 of the present invention since there are data lines DB and DBb and bit lines BL and BLb shown in Figs. 3 and 5; no antecedent basis for "first data" (line 2) and "second data" (line 5); all the recited steps of transferring are not seen to be described in the specification as well as in the drawings of the present invention; the step of transferring the second data from the second sense amplifier to a second bit line after the second sense amplifier is disconnected from the data line is not seen to be described in the specification as well as to be shown in the drawings of the present invention.

Claim 14, the first bit line and the second bit line are not readable on the respective Figs. 3 and 5 of the present invention since there are bit lines BL and BLb in each of memory cell blocks shown in Figs. 3 and 5.

Claim 15, the first bit line are not readable on the respective Figs. 3 and 5 of the present invention since there are bit lines BL and BLb shown in Figs. 3 and 5.

Claim 17, the first bit line are not readable on the respective Figs. 3 and 5 of the present invention since there are bit lines BL and BLb shown in Figs. 3 and 5; the feature "the switching transistor is driven by a first voltage and then driven by a second voltage which is higher than the first voltage" is not seen to be described in the specification as well as to be shown in the drawings of the present invention.

Claim 18, a bit line is not readable on the respective Figs. 3 and 5 of the present invention since there are bit lines BL and BLb shown in Figs. 3 and 5; the feature "the switching transistor is driven by a first voltage and then driven by a second voltage which is higher than the first voltage" is not readable on the respective drawings of the present invention; the feature "wherein data having a voltage drop caused by a threshold voltage of the switching transistor is transferred from the sense amplifier to the bit line by the switching transistor" (lines 3-5) and the feature "wherein data which does not have a voltage drop caused by a threshold voltage of the switching transistor is transferred from the sense amplifier to the bit line" (last paragraph) are not seen to be described in the specification as well as to be shown in the drawings of the present invention.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-4, 7-9, 12-14 and 17-18 are, insofar as understood, rejected under 35 U.S.C. 102(b) as being anticipated by Sakamoto, 6,445,632.

Sakamoto, 6,445,632, discloses in Fig. 2 a memory device comprising:

Regarding claims 1, 4, 7-9, 12-14 and 17:

bit lines BLO and ZBLO which are read on a first bit line;

data lines IOP which are read on a data line;

sense amplifier circuit SAU, in a first memory cell block 2u, which is read on the first sense amplifier;

sense amplifier circuit SAD in a first memory cell block 2u, which is read on the second sense amplifier;

bit line isolation circuit 3ua, controlled by bit line isolation control signal ϕ BIDa, which is read on the switching transistor as recited in claims 7, 12 and 17;

wherein:

when bit line isolation circuit 3ua is brought into non-conductive state (see lines 5-7, column 9), column selection signal CSL is driven into the active state so that latching data of sense amplifier circuit SAU is read (see lines 27-32, column 9) out to the data

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lines IOP which is read on the step of connecting a data line to a first sense amplifier when a first bit line is disconnected from the first sense amplifier; when the data reading with respect to sense amplifier band 2u is completed (see lines 7-10, column 10), data of the memory cells connected to the corresponding bit lines are stored by sense amplifier circuit SAU (see lines 20-23, column 10) which is read on the step of connecting the first sense amplifier when the data line is disconnected from the first sense amplifier; column selection signal CSL applied to column selection gates CGU and CGD may be different (see lines 32-34, column 8), therefore, data stored in second sense amplifier circuit SAD may be read out to data lines IOP at the same time as the first sense amplifier SAU is connected to the bit lines which is read on the step of connecting the data line to a second sense amplifier when the first bit line is connected to the first sense amplifier.

Regarding claim 2:

bit line isolation control signal oBIDa which is read on a common signal;

Regarding claim 3:

when the second sense amplifier circuit SAD is connecting to the second bit lines in the next adjacent memory cell block 2d to store data, the second sense amplifier SAD is disconnected from the data lines IOP;

Regarding claim 18:

each of NMOS transistors T2 in the bit line isolation circuit 3ua, which are read on the switching transistor, having an inherent threshold voltage as well known in the art;

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as shown in Fig. 3, bit line isolation control signal ϕBIDa having a low voltage level which is read on the first voltage and a high voltage level which is read on the second voltage;

since NMOS transistors T2 are N-channel MOS transistors, therefore, they are turned ON by the low voltage level, which is read on the recited first voltage, of the bit line isolation control signal ϕBIDa , data having a voltage drop caused by the inherent threshold voltage is transferred from the sense amplifier SAU to the bit lines by the ON NMOS transistors T2a as well known in the art;

since NMOS transistors T2 are N-channel MOS transistors, therefore, they are turned OFF by the high voltage level, which is read on the recited second voltage, of the bit line isolation control signal ϕBIDa , the data which does not have a voltage drop caused by the inherent threshold voltage is transferred from the sense amplifier SAU to the bit lines by the OFF NMOS transistors T2a as well known in the art.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 5-6, 10-11 and 15-16 are, insofar as understood, rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto, 6,445,632, in view of Kwon et al., 5,973,972.

Sakamoto, 6,445,632, discloses every features except the features as recited in claims 5-6, 10-11 and 15-16.

Kwon et al., 5,973,972, discloses in Fig. 1 the teaching of using transfer gates TG1 and TG2 each comprising a pair of complementary PMOS transistor and NMOS transistor being controlled by respective complementary control signals Y and /Y for connecting the bit lines BL and /BL of memory cell 10 to sense amplifier 60.

It would have been obvious under 35 USC 103(a) to one of ordinary skill in the art at the time of the invention was made to utilize transfer gates TG1 and TG2 in Fig. 1 of Kwon et al., 5,973,972, for the NMOS transistor T2 in Fig. 2 of Sakamoto, 6,445,631, for the purpose of connecting the bit lines BLO and ZBL) of memory cell MC to sense amplifier circuit SAU in Fig. 2 of Sakamoto, 6,445,631.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Takemura et al., 6,944,078, Nakamura et al., 5,905,685, Ooishi, 6,205,071, Kajigaya et al., 4,893,277, and Kajitani et al., 7,102,294.

Response to Arguments

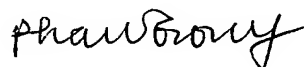
Applicant's request for personal interview, including the attendance of Supervisor Zarabian, prior to examination of this application is denied for the reason that the last Final Office Action of 2/22/06 has been withdrawn.

All of Applicant's arguments in the Remarks of Applicant's request for reconsideration of the last Final Office Action of 2/22/06 are not responded for the reason that the last Final Office Action of 2/22/06 has been withdrawn as requested by Applicant.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to TRONG PHAN whose telephone number is (571) 272-1794. The examiner can normally be reached on M-F (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, AMIR ZARABIAN can be reached on (571)272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



**TRONG PHAN
PRIMARY EXAMINER**